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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,773	09/26/2003	Bunsho Kuramori	030712-13	4336

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,773	KURAMORI ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Drawings

The amendment and drawings submitted on Sep 12, 2005 have been reviewed and considered with the following results:

The examiner has approved the Replacement Sheets. Since they overcame the drawing objections described in the previous Office Action, those objections have now been withdrawn.

The applicants' arguments were not persuasive and the title remains objected to. That objection, and related comments, are described later under their appropriate section.

The amended abstract is objected to for reasons similar to the title. These objections, and related comments, are described later under their appropriate section. Also, some of the amended changes to the abstract created new objections, which are described later.

The amended paragraphs overcame most of the objections described in the previous Office Action, which have now been withdrawn. However, the objection with respect to where VBB actually comes from has not been satisfactorily addressed. Therefore, that objection is maintained, and is repeated later, in the appropriate section.

The rejections of claims 1-6 under 35 U.S.C. 112, first paragraph have been maintained and are repeated later. Associated comments are described under the Response to Arguments section.

The amended claims, and/or comments, satisfactorily overcame the rejections of claim 1 (with respect to first/second levels, and first/third levels), claims 3 and 9 (both with respect to "thinner"), and claims 8 and 10 (both with respect to "The substrate voltage generating circuit"). Therefore, those rejections have been withdrawn. However, the rejections under 35 U.S.C 112,

second paragraph, related to the "input signal" have been basically maintained, with some slight modifications. These rejections, and associated comments, are described later under their appropriate section.

Specification

The title of the invention, a "substrate voltage generating circuit" is still believed to be describing an invention that is neither clearly shown nor disclosed with respect to how it can actually generate a voltage (e.g. VBB) having a third potential lower than the second potential, as described later. A new title is required that is clearly indicative of the invention to which the claims are directed, and which is accurately shown/disclosed within the figures/disclosure. Therefore, it is suggested the title relate to what the examiner believes is the main critical feature of the application: a level shift circuit, with two transistors having thicker gate oxides than two other transistors within the level shift circuit.

The abstract of the disclosure is still objected to because, like the title, the abstract is believed to be describing a substrate voltage generating circuit that is not clearly shown or disclosed, with respect to being able to generate voltage VBB. It is suggested the abstract concentrate on the level shift circuit of the invention. Also, if the level shifting circuit outputs an output signal VBB, how can that output signal have the first and third potential levels since line 4 of the abstract clearly cites "a third potential level VBB"? It is not clear if the applicants' actually mean "in response to the output signal VBB" as recited on line 10 of the abstract, or if --in response to the output signal of a corresponding level shifting circuit--, or --in response to the input signal-- was meant. Corrections and/or clarifications, are required. See MPEP § 608.01(b).

The disclosure remains objected to because of the following informalities: It is still not understood how substrate voltage VBB is transferred to output node OUT.vbb when switch element SW1 is on as described on page 13, lines 14-17. For example, when SW1 of Fig. 1 is turned on, it would be obvious to one of ordinary skill in the art that VSS is coupled to OUT-vbb. Therefore, where does "VBB" actually come from? Related to the above problem, since nodes n1 and n2 are coupled directly to VSS, how can those nodes have substrate voltage VBB outputted from output node OUT.vbb as described on page 15, lines 15-18? Appropriate corrections, and/or clarifications, are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-6 remain rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a level shift circuit, does not reasonably provide enablement for a substrate voltage generating circuit. Therefore, the use of "substrate voltage generating circuit" within the preamble of claim 1 does not accurately identify the circuit being described within the claim. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Although the applicants' own Fig. 1 is identified as a "substrate voltage generating circuit" that apparently generates substrate voltage VBB at its output terminal, the figure and disclosure do not clearly show/disclose how this is actually accomplished. For example, the right terminal of both capacitors c1 and c2, as well as one

terminal from each of NMOS transistors SW1 and SW2, are coupled directly to VSS. Therefore, when the gate of the transistors receives a low signal VBB (through inverters INV1 and INV 2, respectively), the transistors will be off and VSS is not coupled to output terminal OUT_vbb. Also at this time, the left terminal of capacitors c1 and c2 will receive VDD (through inverters INV3 and INV 4, respectively), and would charge up towards VDD via the pull-up section of their respective inverter (e.g. INV 3 or INV 4). However when the outputs of inverters INV 1 and INV 2 transition from VBB to VDD, the gate of the corresponding transistor (e.g. SW1 or SW2) receives VDD, and the transistors turn on, coupling VSS to output terminal OUT_vbb. At this time, the left terminal of capacitors c1 and c2 receive VSS (through the pull-down section of their respective inverter INV3 or INV 4), thus discharging the capacitor's previous charge of VDD towards VSS. Therefore, it is not understood how the claimed invention (e.g. related to the applicants' own Fig. 1) can be a substrate voltage generating circuit that apparently generates a third potential level (e.g. VBB), that is supposedly lower than the second potential level (e.g. VSS), at the output node (e.g. OUT_vbb). Since the circuit within Fig. 1 doesn't appear to actually generate VBB itself, but merely helps control its level (e.g. if VBB becomes more negative than desired, and needs to be raised up towards VSS to bring it back into an acceptable range), what actually generates VBB, and then apparently applies it to node OUT_vbb? Dependent claims 2-6 carry over the rejection from claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants

regard as the invention. It is not clear in claim 1 how the "output node having a third potential level lower than the second potential level" (lines 5-6), actually relates to the output node being connected to the second power supply node (lines 11-12), which is supplied with the "second potential level." For example, when the output node is connected to the second power supply node through the switch circuit, wouldn't the output node have substantially the second potential level instead of the third potential level? Also, since claim 1 is a substrate voltage generating circuit, how does the voltage at the output node relate to the implied substrate voltage the circuit apparently generates? The applicants' use of "an input signal having the first and second potential levels" in claim 1 (line 8), and the use of "the input signal" in claim 2 (lines 3-6) are confusing. Claim 1 appears to imply that the single input signal alternates between the first and second potential levels, and in claim 2 the same single input signal is applied to the gate of the first-fourth transistors. For example, as shown in the applicants' own Fig. 2, and its associated disclosure, the first/second transistors P1/P2 receive complementary input signals, not the same "input signal" as claim 2 implies. Claim 3 has the same type of problem as claim 2, wherein the first/second transistors do not receive the same "input signal" as the limitations on lines 3-6 imply. Both independent claims 7 and 9 have the same single "input signal" related problem as claims 2 and 3 described above (i.e. the first/second transistors do not both actually receive the same "input signal" as lines 2-5 of each of claims 7 and 9 imply). Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 7 and 9 would be allowable if rewritten or amended to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the gate oxide thicknesses of the third/fourth transistors is thicker, or thinner, than from the gate oxide thicknesses of the fifth/sixth transistors as recited within claims 7 and 9, respectively.

Also, claims 8 and 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. These claims depend on claims 7 and 9, respectively, which would be allowable as described above.

Response to Arguments

The applicants' arguments filed Sep 12, 2005 have been fully considered but they are not persuasive. The applicants argue: 1) the title of this invention should be acceptable; 2) the amended abstract improves the level shifting circuits' description; 3) one of ordinary skill in the art knows c1, n1, c2, n2, and VSS affect voltage VBB at output node OUT.vbb; 4) the final output is substrate voltage VBB; 5) various examples show substrate voltage generators; and 6) the input signal has first and second potential levels.

1) Although the applicants identify U.S. Patent No. 6,700,434 as an example having a title "Substrate Bias Voltage Generating Circuit", and then cites the title of the present application should also be acceptable, there are at least two major differences between the patent and the present application with respect to what is being considered a generating circuit. The patent clearly shows, and discloses, a circuit that actually can provide substrate bias voltage

VBB. For example, the pump circuit shown in Fig. 19A can generates voltage VBB. However, none of its capacitors are coupled directly to VSS as the present application's Fig. 1 clearly shows (e.g. see c1 and c2). Therefore, unless the applicants can clearly prove that their circuit (i.e. as presently shown in Fig. 1, and originally disclosed) can actually provide substrate voltage VBB, the title of the present application is either inaccurate, or misleading. This examiner presently believes the applicants' Fig. 1 circuit cannot actually provide voltage VBB at output OUT_vbb that is less than VSS.

2) The changes to the abstract apparently imply that third potential level VBB is actually output by the level shifting circuits, and has first and third potential levels. However, line 4 of the abstract cites "a third potential level VBB", which contradicts VBB having the first potential level. Also, the abstract implies the switch circuit responds to output signal VBB, but not necessarily to the output of the level shifting circuit. Therefore, the abstract is confusing and requires changes to better clarify the claimed invention.

3) The applicants argue that one of ordinary skill in the art knows c1, n1, c2, n2, and VSS affect voltage VBB at output node OUT.vbb (e.g. see the applicants' Fig. 1). This is true up to a point. However, since nodes n1 and n2, coupled to capacitors c1 and c2, respectively, are both coupled directly to VSS (e.g. ground), it appears that when their corresponding switch (e.g. SW1 or SW2) is conducting, voltage VBB on node OUT.vbb will be pulled towards VSS. Therefore, it is still not known how VBB can actually be generated by the circuit shown in Fig. 1.

4) The applicants argue that the specification clearly describes the level shift circuits, and their cooperation with other features to generate substrate voltage VBB. Although the examiner agrees the level shift circuit descriptions are clear and sufficient, nothing in the figures, the

disclosure, or the amendment's comments, clearly shows or describes how substrate voltage VBB is actually generated. The examiner has no problem understanding how the output of a level shift circuit, or an inverter, can have a high level at VDD and a low level at VBB. However, how voltage VBB (less than voltage VSS) can actually be generated (e.g. by capacitor c1, node n1, voltage VSS, and switch SW1 of Fig. 1) is never clearly described. Unless there is some type of blocking element (e.g. a diode or switching element) coupled between the node and voltage VSS, that node will always be maintained at voltage VSS because they are directly coupled to each other. To get a voltage lower than VSS from the presently shown/disclosed circuit, this examiner believes voltage VBB must be generated externally (e.g. outside of the circuitry shown in Fig. 1), and then applied to output node OUT_vbb, and to the level shift circuits 101 and 102, of Fig. 1. Until the applicants can clearly prove otherwise, this examiner strongly believes the circuitry (as presently shown) in Fig. 1 will not be able to generate substrate voltage VBB as the output voltage. If the applicants believe an affidavit will confirm how the originally shown/ disclosed substrate voltage generating circuit actually generates voltage VBB, then the examiner respectively requests the affidavit. However, since the operation of the level shifting circuits and inverters are clearly understood, it is suggested the affidavit clearly focus on the operation of how substrate voltage VBB is actually generated. For example, step-by-step operation of how capacitor c1, node 1, voltage VSS, switch SW1, and output terminal OUT-vbb function together to be able to provide voltage VBB at a level less than VSS would be the most helpful.

5) Although the applicants provided seven examples of substrate voltage generators to the examiner for additional background (e.g. see page 15 of he amendment), those examples are not

considered relevant to the present application's substrate voltage generator. Four of the references do not even show a capacitor with one of its terminals coupled to VSS (or ground), and one of these references (i.e. Jeon) shows only a generic type block identified as a charge pump. One (i.e. 5,905,582) of the other three references does not even show a substrate voltage generator, and since its inventor Hirai does not correspond to Gans et al. (i.e. the inventor according to the applicant), it is believed the patent number has at least one typo within it. Neither of the other two remaining references clearly shows a capacitor directly coupled to VSS, wherein the capacitor is actually part of the substrate voltage generator itself. For example, although the reference of Ryu shows capacitors coupled to VSS, they are all in a ring oscillator that provides a clocking signal to a substrate voltage generator (e.g. a charge pump), and the capacitors shown in Chern's Fig. 3 are related to capacitor C1, and are not actually part of the charge pump itself (e.g. see 24 or 64 shown in other figures). Therefore, if the applicants plan to submit any more references for the examiner to spend time reviewing, it is suggested the references actually be relevant to a substrate voltage generating circuit having at least one capacitor coupled directly to VSS, wherein that direct connection is also coupled to one side of a switching element having its other side coupled to an output node that apparently provides voltage VBB.

6) The examiner will agree that an input signal having first and second potential levels is understood. For example, such a signal typically means a single signal that alternates between the two levels. However, an input signal with first/second potential levels does not mean there are two separate signals, such as complementary signals. As presently recited and understood within independent claims 7 and 9, all four transistors receive (e.g. have their gates coupled to)

the same "input signal". This is misleading and confusing. Using the applicants' own Fig. 1 as an example, transistors P1 and N1 both receive input signal IN, and transistors P2 and N2 both receive input signal /IN. Although these signals are complements of one another, they are not the same input signal. [Note: The paragraph on page 3 of the amendment (corresponding to a paragraph bridging pages 5 and 6 of the disclosure) clearly discloses first and second input signals (e.g. see lines 3-5), thus supporting the examiner's belief that the implied single "input signal" of at least claims 7 and 9 should be clarified better (e.g. as first and second input signals).]

For the reasons described above, the rejections described within this Office Action, and within the previous Office Action, are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations.

Prior Art

The two references on the accompanying PTO-892 are cited for interest and documentation purposes only. The six transistor circuit structure shown in Fig. 2 of Kamata corresponds to the applicants' own Fig. 3; and the six transistor circuit structure shown in Fig. 12B of Koyama et al. corresponds to the applicant's own Fig. 2. However, Kamata does not clearly show or disclose anything about the transistors' thicknesses, sizes, or thresholds; and Koyama identifies all the transistors as thin film transistors (i.e. TFTs). Therefore, even though these references show circuit structures that match the applicants' circuit structure, the references lack the thickness differences of the first and second gate oxide films, with respect to the third/ fourth transistors and the fifth/sixth transistors, as recited within independent claims 7 and 9.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T.L.E

Terry L. Englund

16 November 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Approved
11.16.05
TLE

FIG. 2

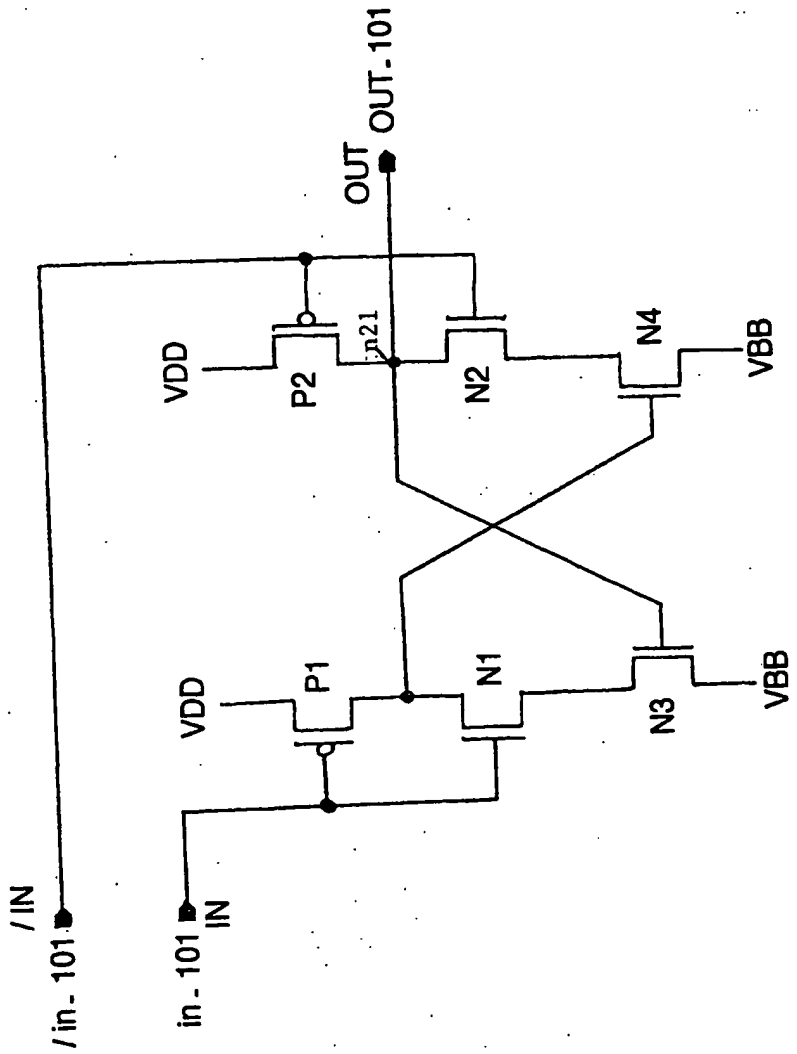

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FIG. 3